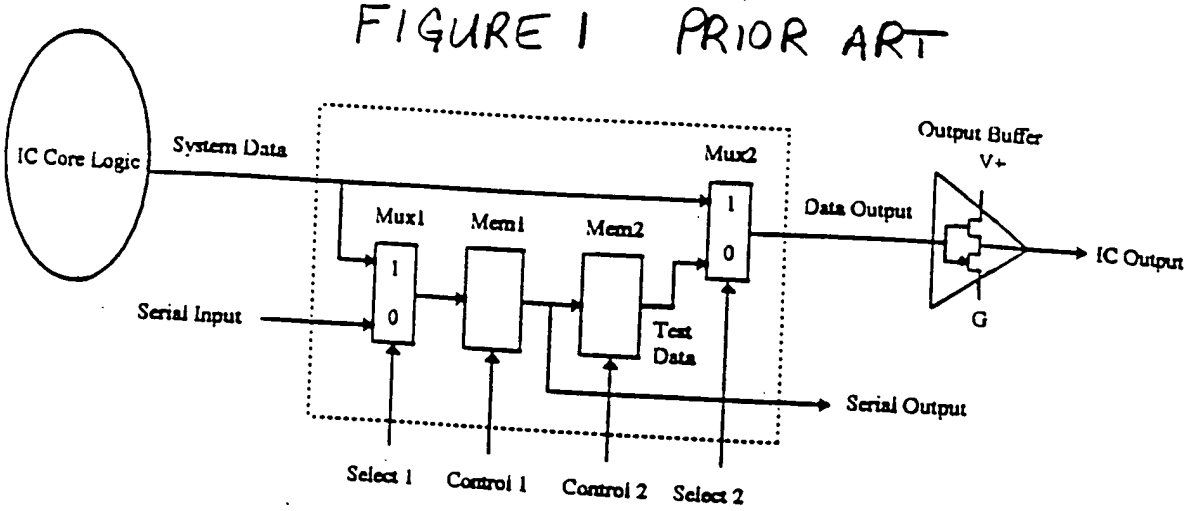
FIGURE 1 PRIOR ART



Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0CCCCCCC00
Control 2	00000000C0	00000000C0	0000000000
Select 2	1111111111	0000000000	0000000000

TIME

Figure 1A

PRIOR ART

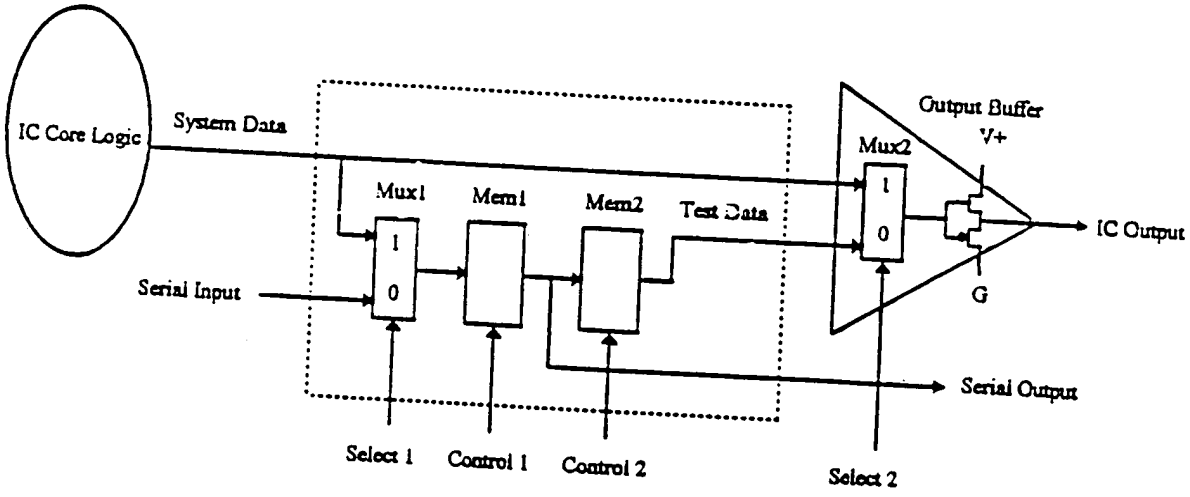


Figure 2

PRIOR ART

FIGURE 3 PRIOR ART

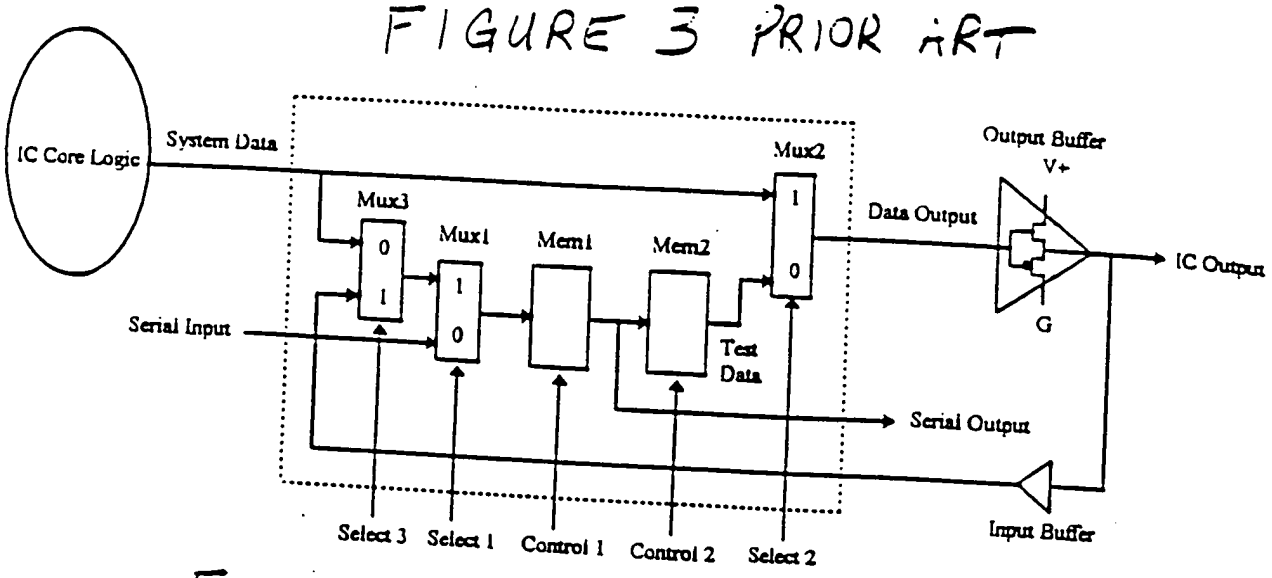


FIGURE 3A PRIOR ART

Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0CCCCCCC00
Control 2	00000000C0	00000000C0	0000000000
Select 2	1111111111	0000000000	0000000000
Select 3	0000000000	1111111111	0000000000

TIME

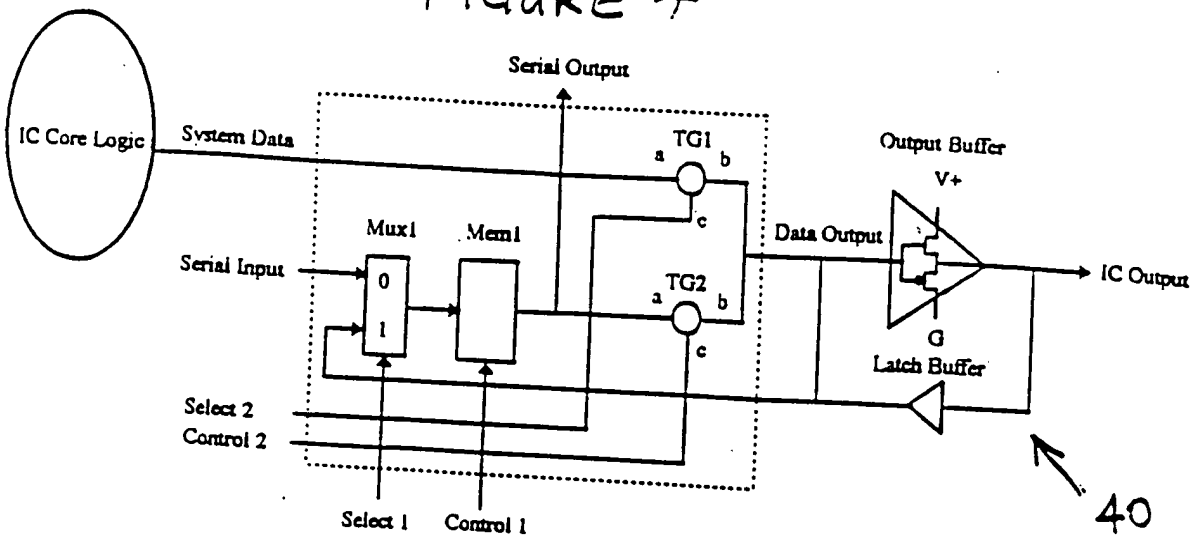
Operation	Extest1	Extest2	Extest3
Select 1	0100000000	0100	0100000000
Control 1	0CCCCCCC00	0C00	0CCCCCCC00
Control 2	00000000C0	00C0	00000000C0
Select 2	0000000000	0000	0000000000
Select 3	1111111111	1111	1111111111

Figure 3 B

TIME

PRIOR ART

FIGURE 4



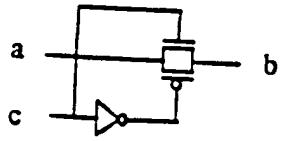
Operation	Sample	Extest
Select 1	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00
Control 2	0000000000	00000000C0
Select 2	1111111111	0000000000

FIGURE 4A → TIME

Operation	Extest
Select 1	0100000000
Control 1	0CCCCCCC00
Control 2	1000000011
Select 2	0000000000

Figure 4B → TIME

Transmission Gate used for TG1 & TG2



Tristatable Buffer used for TG1 & TG2

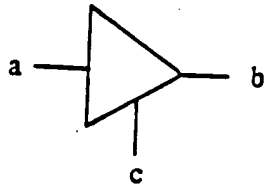


Figure 5

FIGURE 6

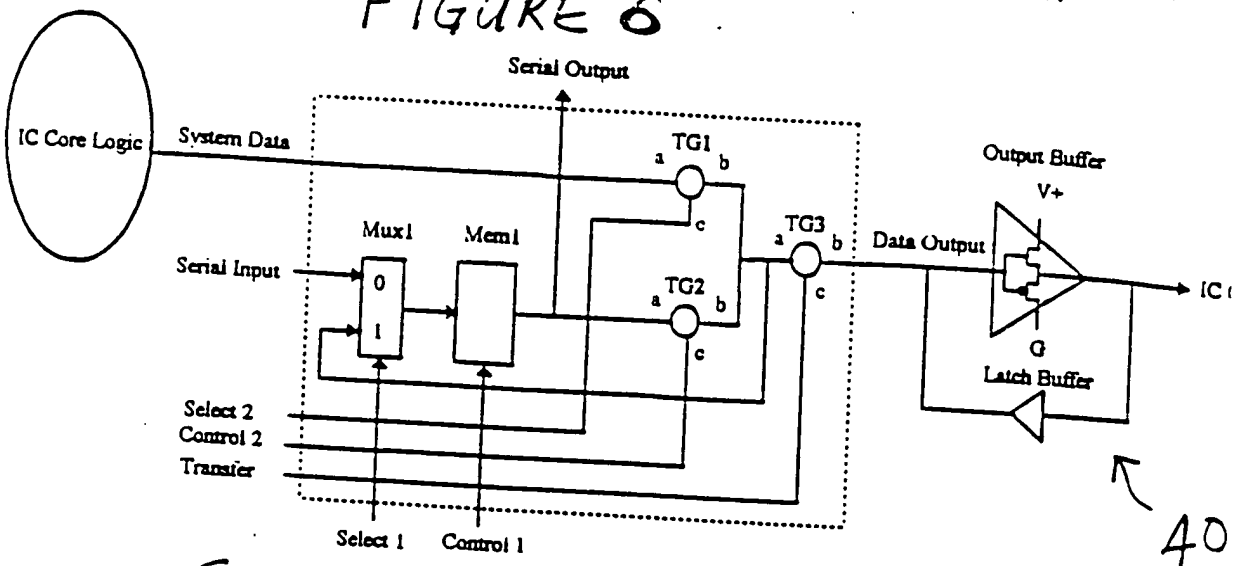


FIGURE 6A

Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0CCCCCCC00
Control 2	0000000000	00000000C0	00000000C0
Select 2	1111111111	0000000000	0100000000
Transfer	1111111111	01000000C0	00000000C0

TIME

Operation	Extest	Intest
Select 1	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00
Control 2	1000000011	1000000011
Select 2	0000000000	0100000000
Transfer	1100000011	1000000011

Figure 6 B

TIME

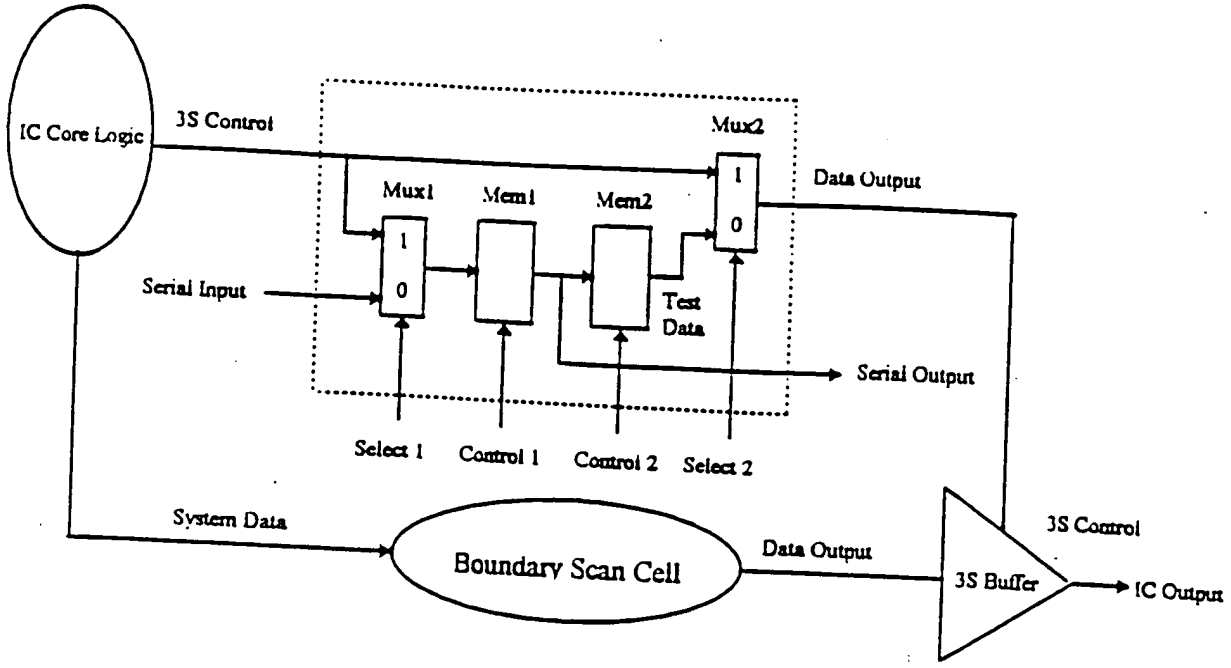


Figure 7

PRIOR ART

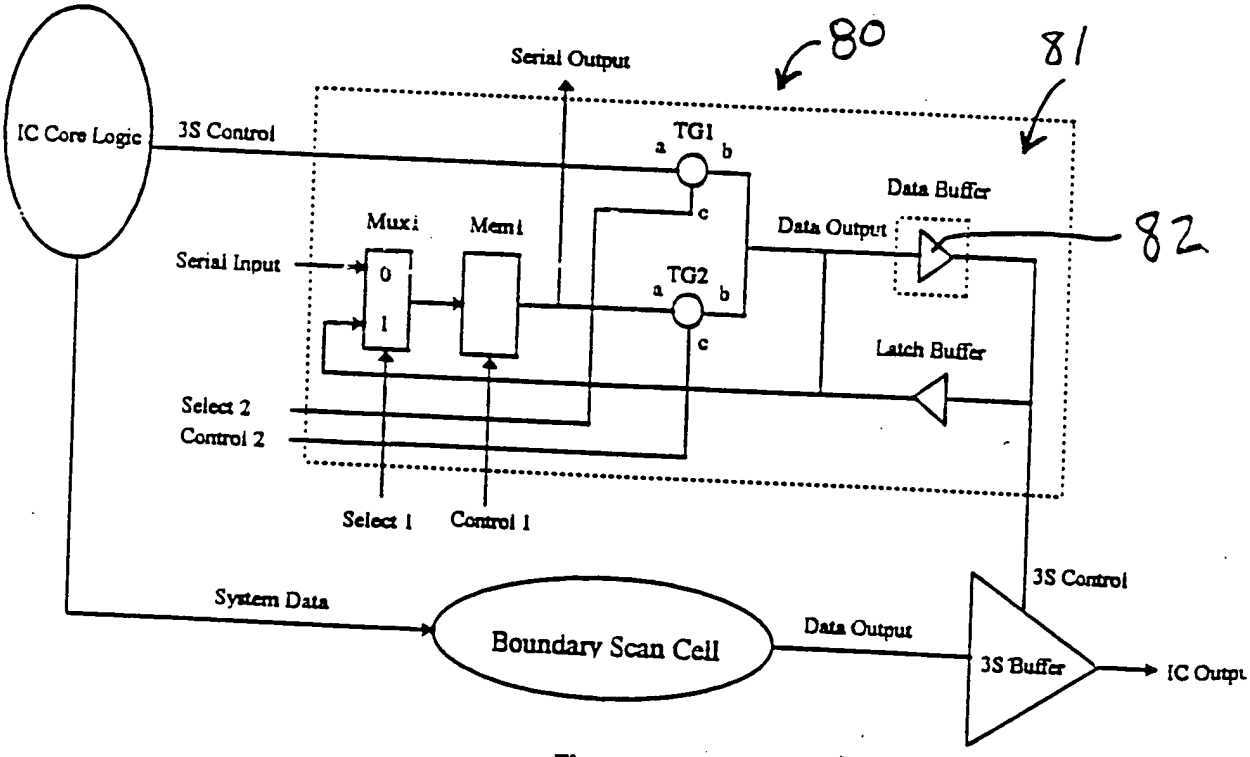


Figure 8

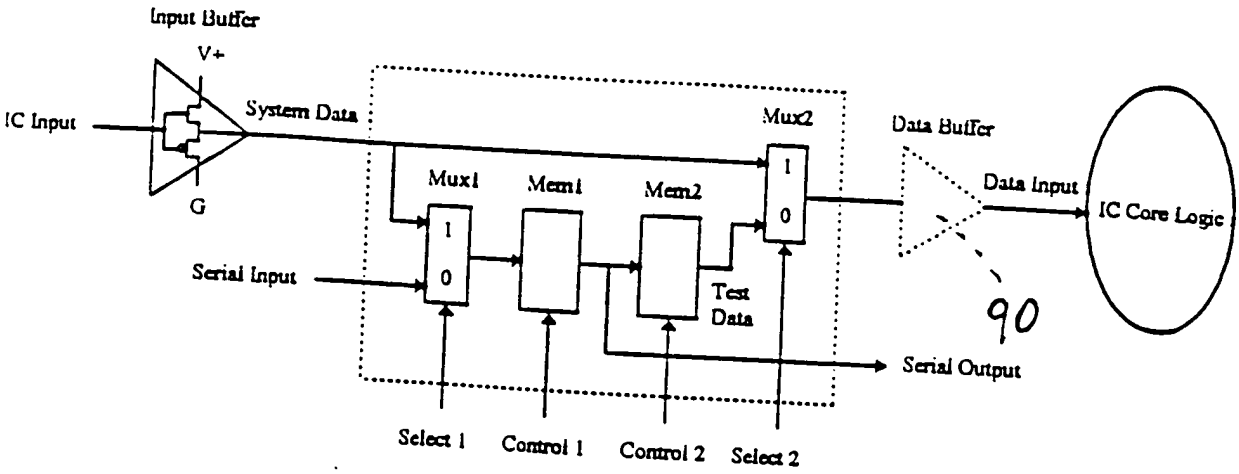


Figure 9 PRIOR ART

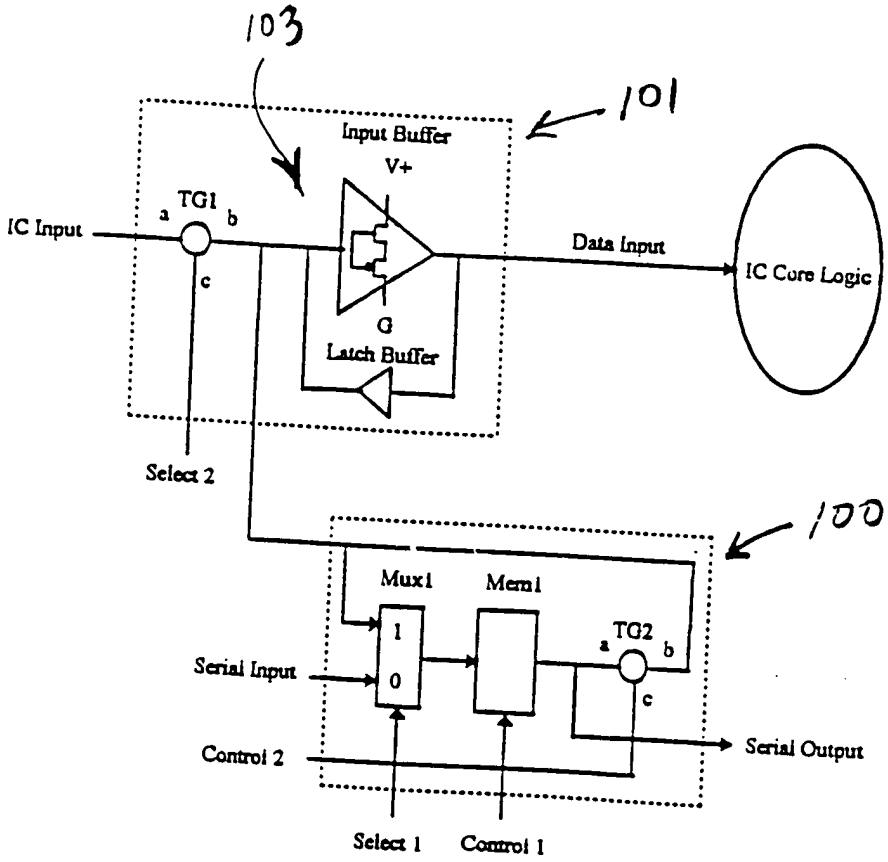


Figure 10

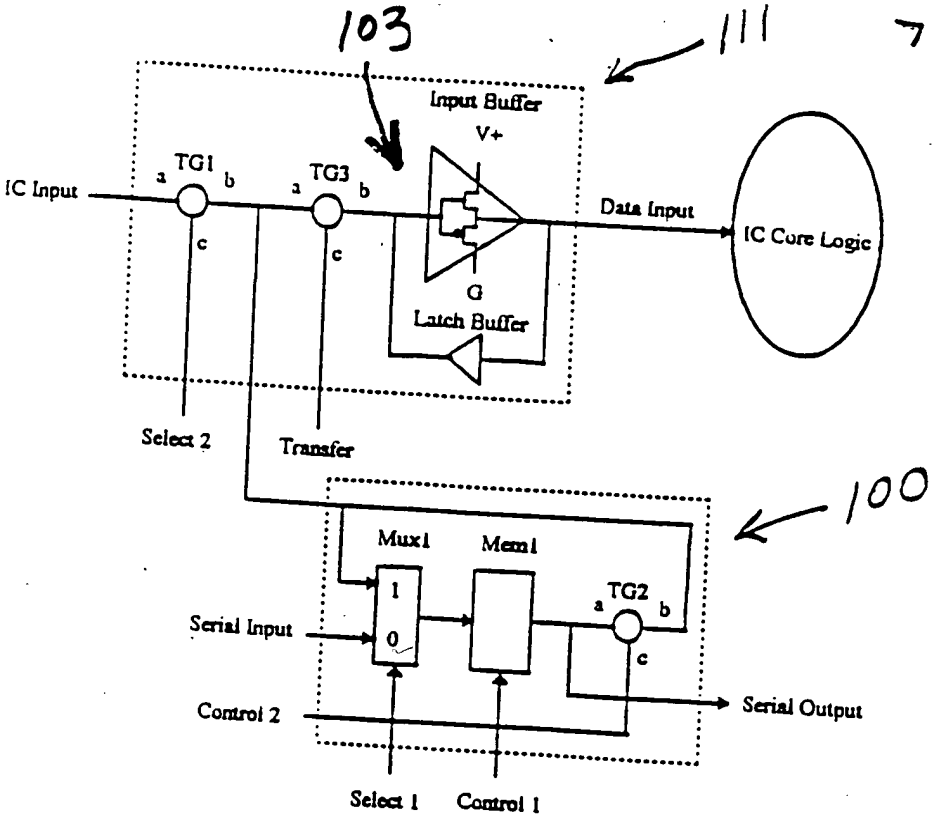

103
111
Input Buffer
V+
IC Input
TG1
a
b
c
TG3
a
b
c
Data Input
IC Core Logic
G
Latch Buffer
Select 2
Transfer
100
Mux1
Mem1
1
0
TG2
a
b
c
Serial Input
Control 2
Serial Output
Select 1
Control 1

Figure 11

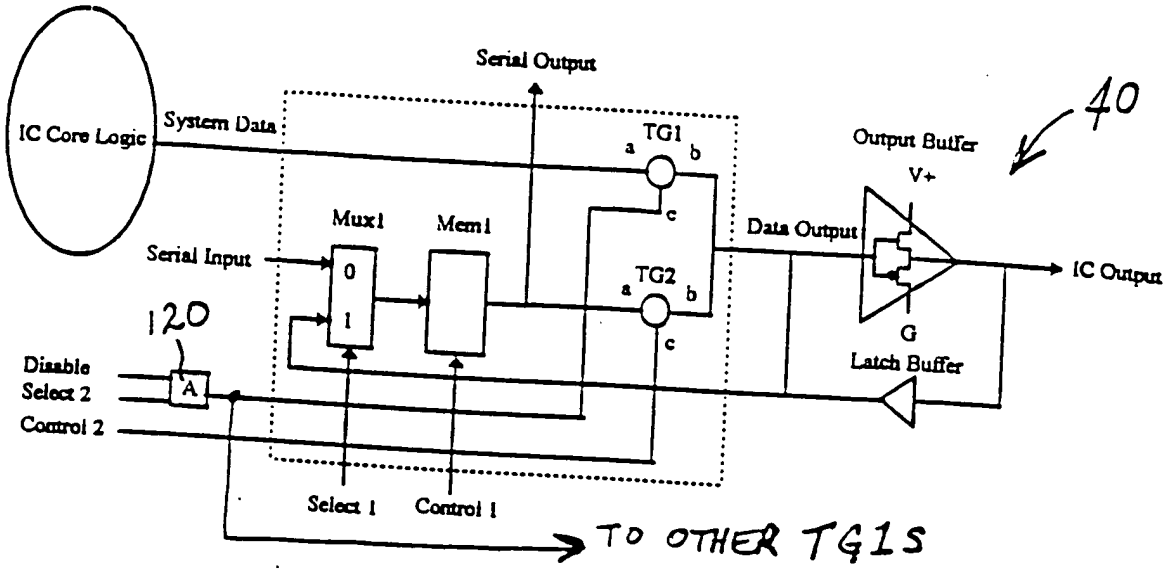


FIGURE 12

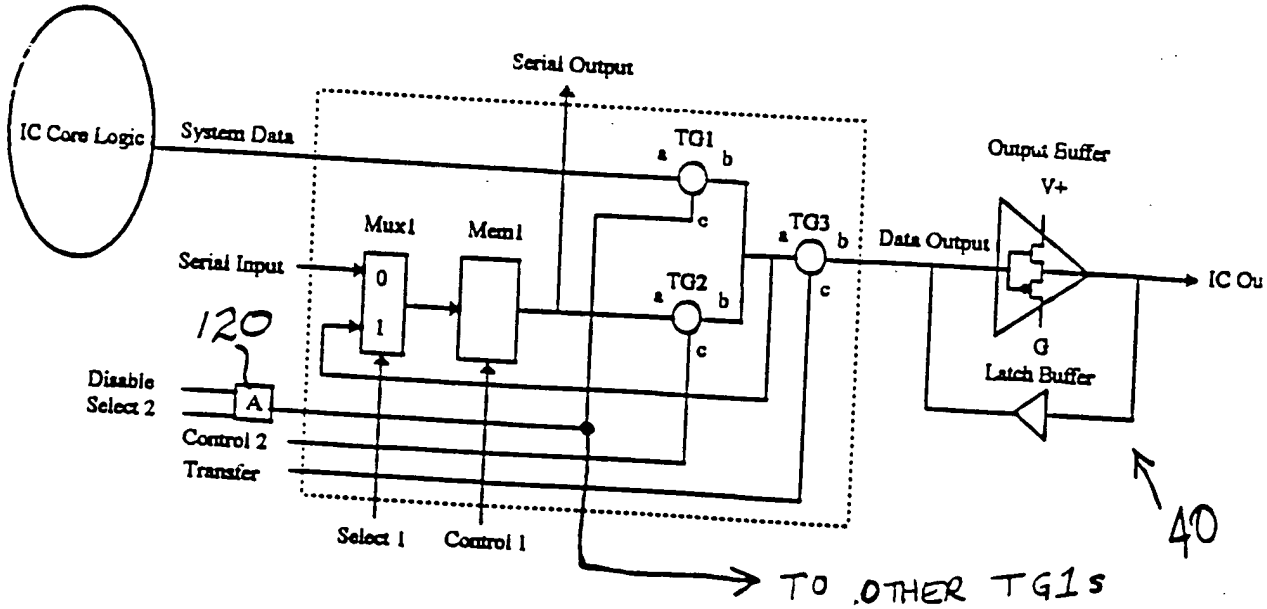


Figure 13

Figure 14

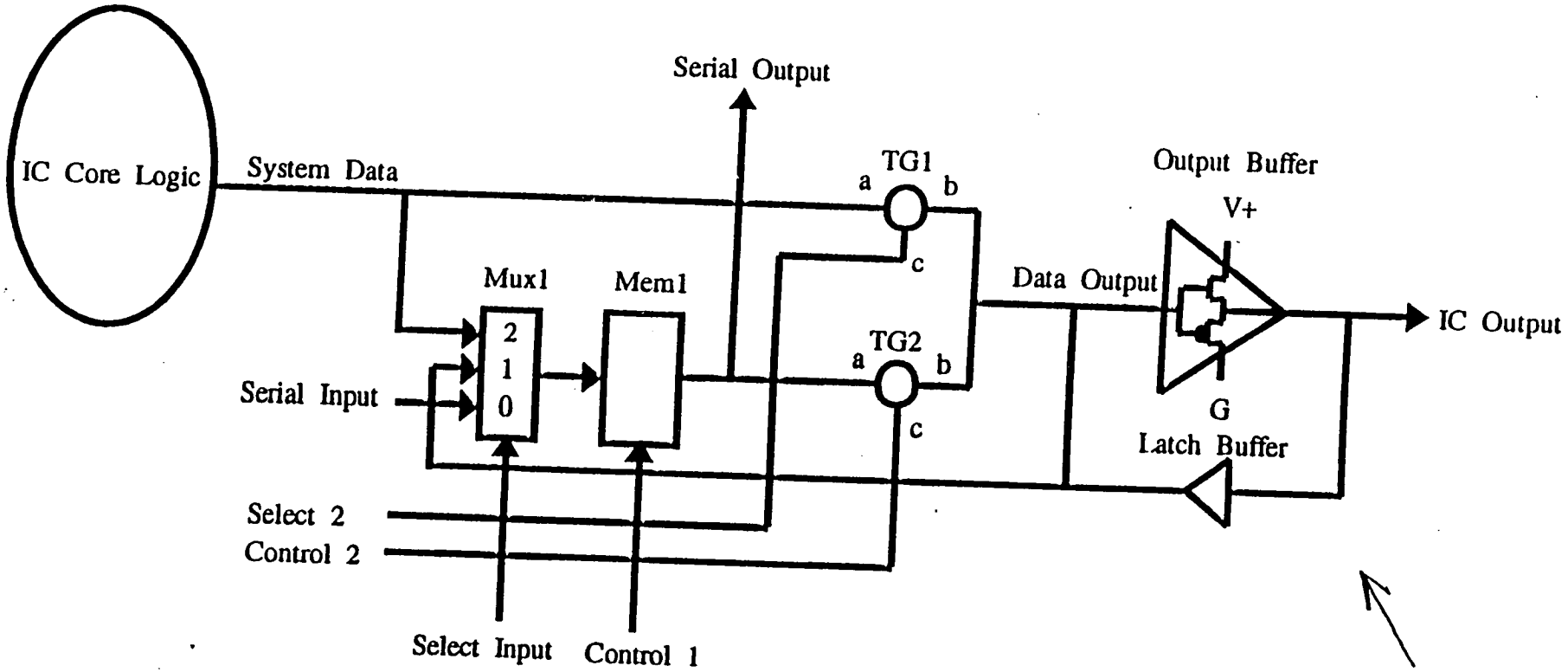

IC Core Logic
System Data
Serial Output
TG1
a
b
c
Output Buffer
V+
Mux1
Mem1
Data Output
IC Output
2
1
0
TG2
a
b
c
Serial Input
G
Latch Buffer
Select 2
Control 2
Select Input
Control 1
40

Figure 15

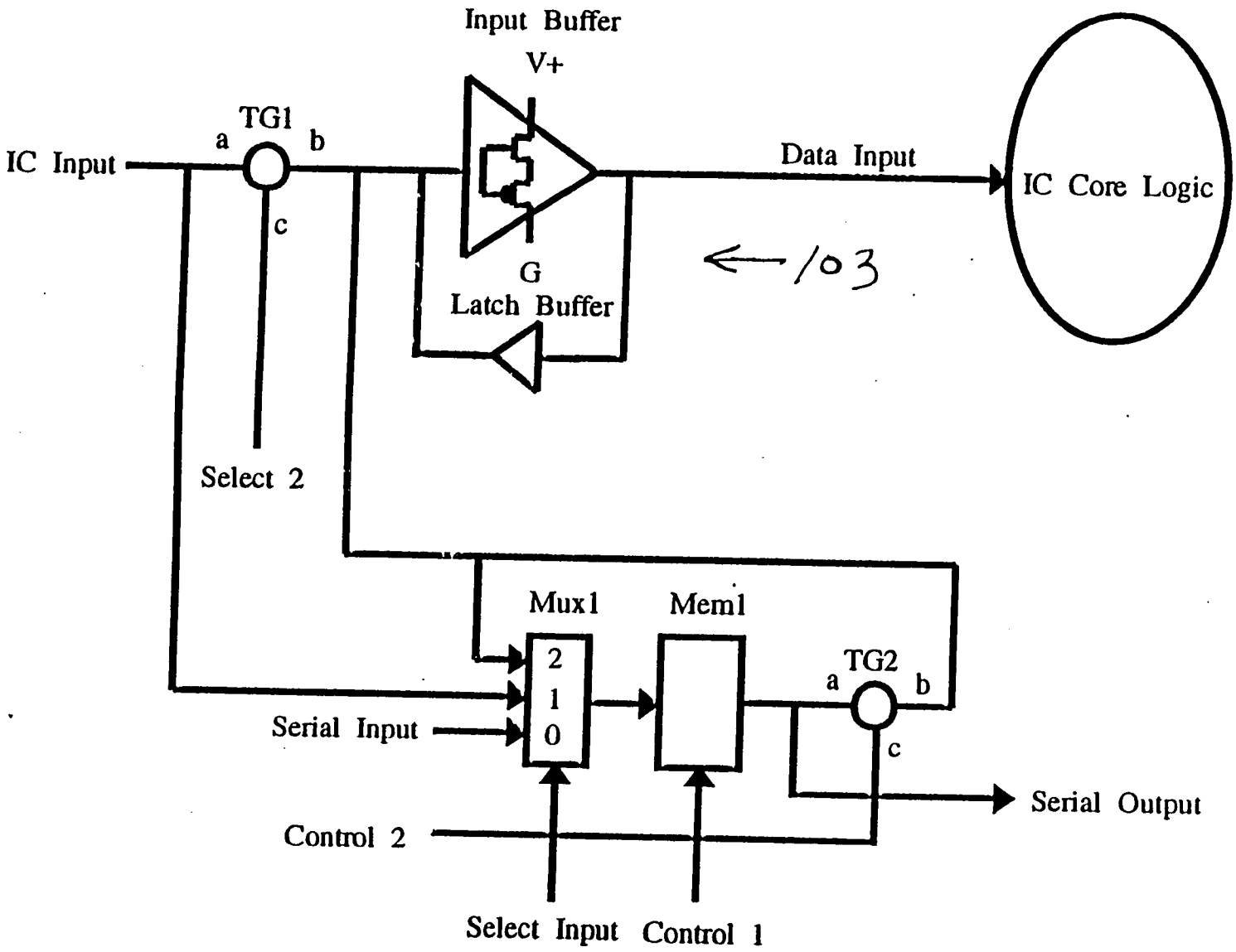
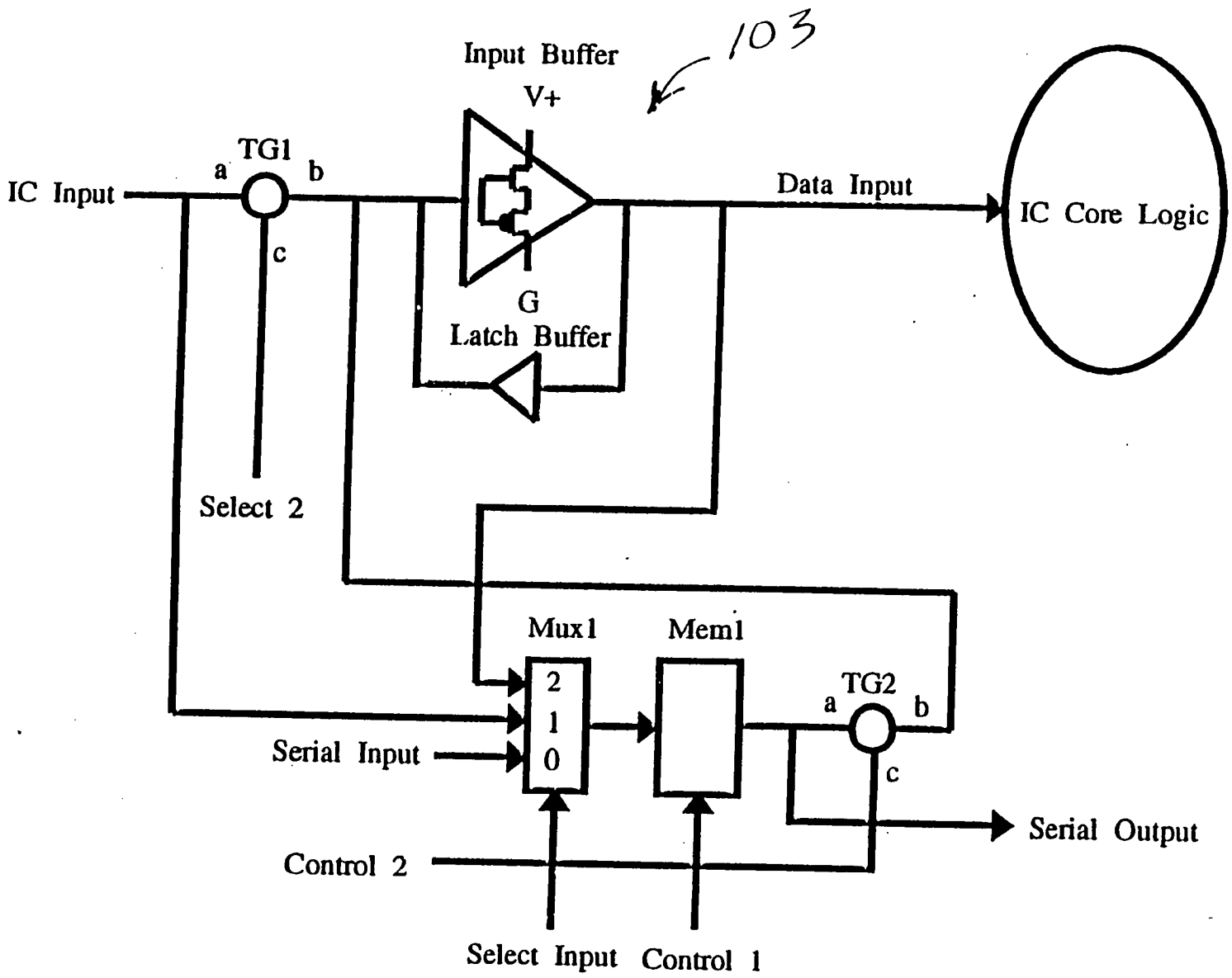

Input Buffer
V+
TG1
a
b
IC Input
c
Data Input
IC Core Logic
G
Latch Buffer
103
Select 2
Mux1
Mem1
2
1
0
TG2
a
b
Serial Input
c
Serial Output
Control 2
Select Input
Control 1

Figure 16


103
Input Buffer
V+
TG1
a
b
c
IC Input
Data Input
IC Core Logic
G
Latch Buffer
Select 2
Mux1
Mem1
TG2
a
b
c
2
1
0
Serial Input
Serial Output
Control 2
Select Input
Control 1